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A 12-BIT 250 MS/S SINGLE-CHANNEL PIPELINE ADC WITH 81 DB SFDR IN 0.13 UM CMOS

Abstract. *A 12bit 250-MS/s pipeline ADC is presented and fabricated in 0.13um CMOS process. A power efficient bootstrap switch with a buffer is proposed for high speed considerations. It utilizes a source follower to insulate the residue amplifier and the large capacitor in the bootstrap switch. Techniques of lightening load capacitance of each stage are proposed to speed up the corresponding residue amplifiers (RA). A clock generator and optimized timing are proposed to achieve low jitter and improve sampling linearity by saving more time for the input switch. The reference buffer and clock buffer are both fully integrated. The signal-to-distortion-and-noise-ratio (SNDR) is evaluated adopting a proper scheme and verified by the measured results. The measured SNDR is 63 dB and spurious free dynamic range (SFDR) is 81dB with 39 MHz. The core area is 2 mm^2 and the ADC consumes 160 mW at 1.3V.*

Keywords: pipeline ADC; bootstrap switches; reference buffer; clock buffer; timing

Introduction

In recent years, mobile communication systems require high performance ADCs to achieve over 80dB of SFDR at 100-300MS/s. Pipeline ADCs are the proper architecture of choice in such applications due to the balance of speed, resolution and power [1]. Time interleaved architectures have been commonly used to realize 250MS/s. However, these structures suffer from offset, gain, timing and bandwidth mismatches, which introduce spurs that limit the SFDR performance. Amplifier-sharing or capacitor-sharing is an effective way to improve the power efficiency of pipeline ADCs, however, the memory effects and cross-talk between successive stages degenerate the AC performance as well [2]. Switch-RA technique is also inadequate for high speed applications because of its turn-on time [3]. The 12 bit 250MS/s ADC in this paper is designed without the above techniques. A bootstrap switch with a buffer is proposed to save power. The load capacitance of each stage is also lightened to speed up the settling of residue voltages. A clock generator with low jitter is proposed and the timing of the ADC is optimized to improve sampling linearity. Based on PSS and Pnoise tools, the noise contributions of multiplying digital-to-analog (MDAC) and clock buffer are easily simulated. The ENOB is then easily calculated and further verified by the factual chip.

Circuit Design

ADC architecture

Fig. 1 illustrates the block diagram of the proposed ADC with a dedicated sample-and-hold amplifier (SHA), 11 pipeline stages and one 2-bit flash ADC. The flip-around S/H and 1.5bit/stage MDAC have the largest feedback factor, which is beneficial for fast settling of the residue. The ADC core works under 1.3V power supply rather than the traditional 1.2V without increasing the obvious power. The power consumption for a single-stage OTA is as the following equation [4]:

$$P \propto \frac{kT \times SNR}{\alpha V_{dd}} \quad (1)$$

When the power supply of the RA raises by 100mV, the overall power consumption decreases actually. Additionally, the switch-capacitor part contributes plenty of power consumption as well. The on-resistance of a

MOS switch is:

$$R_{on} = \frac{1}{kC_{ox}\frac{W}{L}\times(V_{GS}-V_{th})} \quad (2)$$

V_{GS} is usually near V_{dd} when the switch is bootstrapped, and W/L could be decreased when V_{dd} increases for the same R_{on}. As a result, the decreased average current due to smaller size consumed by the switch could offset the 100mV power addition. Furthermore, smaller sizes mean less parasitic capacitance which is beneficial for linearity.

The sampling capacitor of the S/H and the first stage are both 3pF. The capacitors and sizes of RAs are scaled down by 2 in the succeeding stages. The last six stages all use the same sizes to shorten the design schedule. The input span is 1.2Vp-p, which is enough for 12 bit design. Low jitter clock buffer and high speed reference buffer are both fully integrated.

Proposed bootstrap switch

Bootstrap switches are widely used to reduce signal distortion by keeping the gate-source voltage of the sampling switches constant. The generic principle of bootstrap is to apply an on-chip capacitor as a battery. In one phase, this capacitor is charged to V_{dd} and in the other phase redistributes its charge to the gate of input transistor. However, parasitic capacitors also participate in the process of this redistribution, which makes the gate-source voltage less than the ideal V_{dd}. Hence, large capacitor is usually used in the bootstrap circuit. Nevertheless, large amount of capacitor overloads the preceding stage and slows down the signal settling.

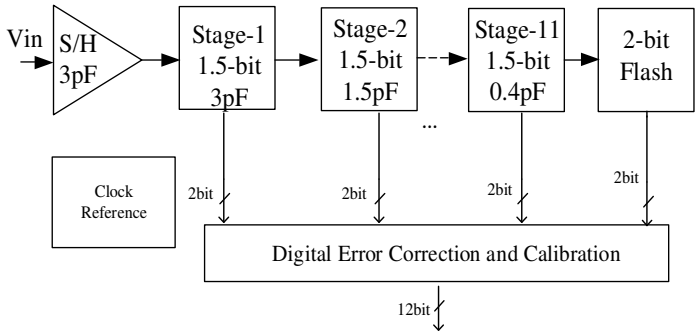

Figure1 – Block diagram of proposed ADC

In the previous work [5] a source follower was inserted to buffer the input and the preceding stage faced relatively small capacitor. A capacitor level shift was used to cancel the dc voltage loss by the source follower. In this paper, a simple low threshold transistor is used as a source follower while causing little dc voltage loss. Fig. 2 shows the proposed bootstrap circuit. In this way no extra capacitor is needed and hence saves area and power. With the simple buffer the preceding stage confronts relatively smaller loads. A deep N-well transistor is used as an input switch to shield itself from the substrate noise. What's more, the bulk terminal is connected to source in the sampling phase to cancel the back-gate-effect and thus improves the sampling linearity. In the amplifying phase, the bulk is connected to the ground supply to make sure that every PN junction is reverse-biased. The proposed bootstrap switches are used in the first 5 stages and in the S/H the source follower is unnecessary due to the strong drive capability outside.

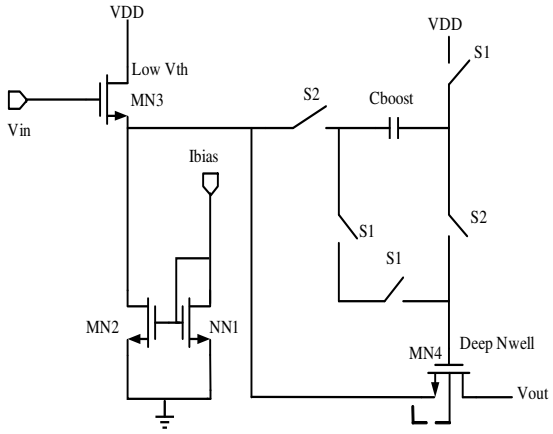

Figure – 2 Proposed bootstrap switch

Way of lightening load capacitors

The operation speed of pipeline ADC relies mainly on the speed of the RA in each MDAC which is determined by a function of W/L and load capacitance [6]:

$$BW_{max} \propto f(W_{opt}) = \frac{\sqrt{2uI\frac{W_{opt}}{L}}}{C_{ox}W_{opt}L+C_l} = \frac{1}{L}\sqrt{\frac{uI}{2C_l}} \quad (3)$$

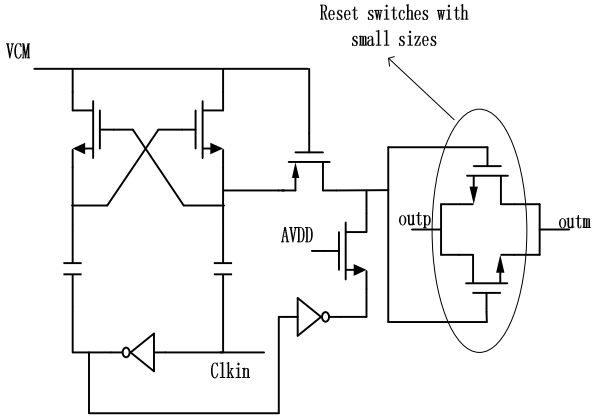

Figure 3 – Bootstrapped reset switches

In the function of maximum bandwidth of the RA is derived and shown here in equation (3). When the power budged is set, the BW_{max} won't improve by increasing W/L blindly. W/L of the input transistors has an optimum value as shown [6]:

$$W_{opt} = \frac{C_l}{C_{ox}L} \quad (4)$$

From Eq. 3 and Eq. 4, minimum load gives minimum W_{opt} and maximum bandwidth with the length

L limited by process and current I limited by total power budget. The load capacitor C_l consists of the input capacitors of next stage and the corresponding parasitic, in which sampling capacitors are limited by kT/C noise and mismatches. The capacitance of the input of sub-ADC and reset-switches-induced parasitic still contributes about 25% of the load. Inter-metal coupling capacitors and interleaved layout floor plan are used here to realize low value capacitors. Reset switches of the output of OPAMPs are bootstrapped and quite small W/L is used to lower the induced parasitic capacitance as shown in Fig. 3. The two same NMOS transistors are connected in parallel with the source and drain terminals in opposite direction and thus make the same parasitic for the output. With the above two techniques C_l is lowered by 15%, which is essential in high speed applications.

Design optimization of the clock buffer and timing

Clock jitter would degenerate the performance of the ADC especially when handling high input frequencies. Clock jitter could be periodic or random, which comes from the signal source outside the chip and the on-chip clock generator. The modern advanced signal source could give a relatively pure sine wave which is often band-pass filtered further more and finally brings less than 100 fs RMS jitter. This sine wave is amplified and buffered to form a square wave by a clock buffer. It is imperative to simulate and calculate the jitter noise precisely and then minimize it. The jitter noise is given as [7]:

$$N_j = \left(2\pi f_0 A_{rms} t_j\right)^2 \qquad (5)$$

It is essential to keep the SNDR above 62 dB(ENOB=10bit) for IF sampling, for instance, 500MHz input frequency for a 1.2Vp-p signal. As a result, we need.

The jitter noise is given as:

$$t_{j,total} < 216\, fs \qquad (6)$$

The clock generator is shown as in Fig. 4. The internal jitter noise is mainly caused by thermal noise and 1/f noise of the transistors. The sine wave should cross the zero point quite fast to reduce the uncertainty induced by various noise sources.

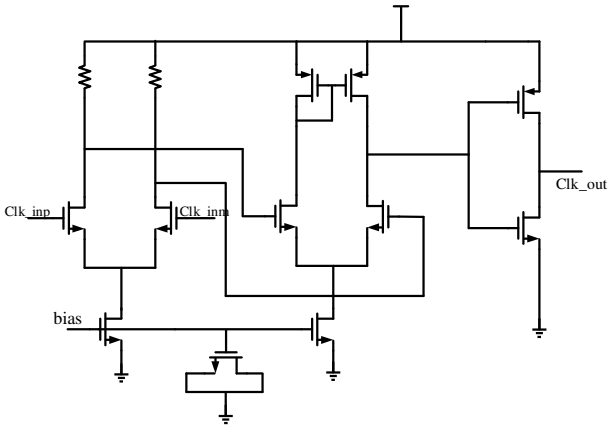

Figure 4 – Schematic of clock generator

Large current is consumed by the first two stages to make fast crossing. Decoupled capacitors are used to filter the bias noise and stabilize the dc current. By using PSS and Pnoise the RMS jitter is about 120 fs. The noise from power supply also influences the purity of the clock. In this work a dedicated LDO chip is used for the clock generator on the PCB to provide a clean power.

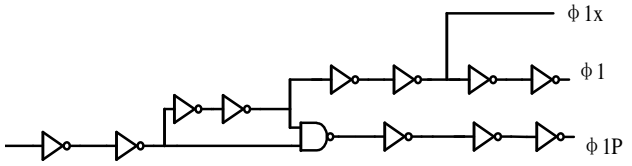

Figure 5 – Schematic of improved local clock

Additionally, quantities of on-chip decoupled capacitors are applied as well. Key transistors are shielded from noise in layout. The noise model of power supply is hard to make precisely. LDO and on-chip capacitors could restrain quite low and high frequency interference. Intermediate frequency like several MHz noise may still exist and is evaluated by eye-diagram. The eye-diagram of the sampling clock with the power supply disturbed by 10MHz 1mV Vp-p interference (relatively conservative estimation) is simulated. The data of the eye-diagram is peak-to-peak and then transformed to RMS format, which is 65 fs. Although this estimation is not that precise, the order of magnitude is still correct and can be used to assess the final jitter noise. Three noise sources give us the total jitter noise: noise precisely and then minimize it. The jitter noise is given as:

$$\sqrt{100^2 + 1200^2 + 65^2}\, fs = 169\, fs \qquad (7)$$

The clock is further buffered locally as shown in Fig. 5 and its outputs are shown in Fig. 6.

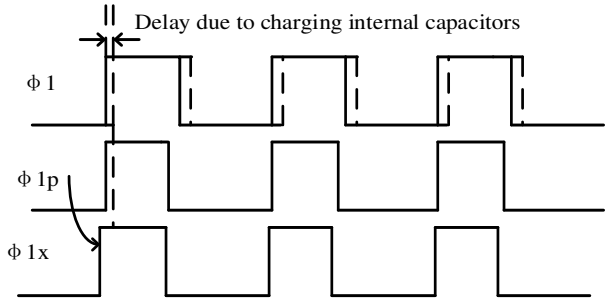

Figure 6 – Output of local clock generator

S1 is from the global non-overlapping clock. P1 is cut down ahead of time for bottom-sampling trough inverters and a NAND gate. The bootstrap switch usually experiences an extra delay due to the process of charging capacitors and hence φ1 actually rises later than P1, which is shown as the dotted line of φ1 in Fig. 6. This extra delay wastes some sampling time and thus is inferior to the sampling linearity. The proposed scheme utilizes φ1x as the clock of the bootstrapped switches, which rises ahead of φ1p.

Post simulation is executed for many PVT corners to ensure that φ1p falls ahead of φ1x, resulting in correct bottom sampling. The simplified and improved timing saves about 60 ps for sampling.

Measurement Results

The proposed ADC has been fabricated in TSMC 0.13-μm CMOS process and its chip core area is 1 mm * 2 mm. Fig.7 shows the microphotograph of the proposed ADC. Table 1 lists the noise contribution of each key module, simulated by the PSS and Pnoise tools.

Table 1 – ***Simulated noise of each key module***

Bits	12
Full scaled input	0.4243V(rms)
Quantized noise	84.6uV(rms)
Jitter noise	56.3uV(rms)
Input cap noise of S/H (input referred)	54.1uV(rms)
S/H OPAMP and stage1 cap noise (input referred)	70uV(rms)
Stage1 OPAMP and stage2 cap noise (input referred)	42uV(rms)
Stage2 OPAMP and stage3 cap noise (input referred)	18uV(rms)
Stage3 OPAMP and stage4 cap noise (input referred)	10uV(rms)
Stage4 OPAMP and stage5 cap noise (input referred)	8uV(rms)
Stage6 OPAMP and stage7 cap noise (input referred)	6uV(rms)
Reference noise (input referred)	25uV(rms)
Settling and DC accuracy	102uV(rms)
Total noise (input referred)	177.4uV(rms)
ENOB	10.9 bit
SNDR	67dBFS

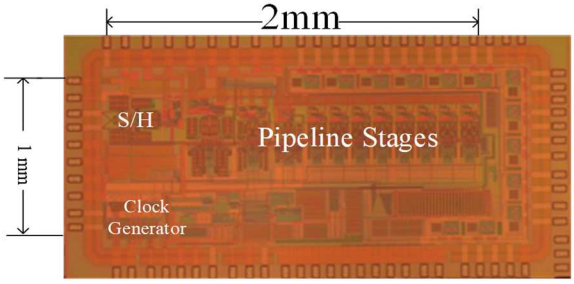

Figure 7 – Chip photograph of proposed ADC

Both input signal and clock signal are generated by the pure signal sources, which are then filtered by high-quality Band-pass customized filters. Two baluns are adopted to transform the single-end signal to the differential one. To minimize the phase and amplitude imbalance, a pair of baluns are connected back-to-back. The common mode level is defined by the buffer integrated in the chip. Working at 250 MS/s, the ADC achieves 80 dB SFDR and 62.64 dB SNDR with Nyquist input and 81 dB SFDR and 63.49 dB SNDR with about 39.1 MHz input, as shown in Fig. 8. The total power consumption of one single core is about 160 mW. The measured SNDR is about 3 dB inferior to the evaluated one from table 1, mainly because the parasitic from the layout design and substrate noise of the chip as well as the noise from the PCB.

The symbol * means only single-channel.

Table 1 summarizes and compares the performances of the proposed ADC with other works. The Waldon figure of merit (FOM) is expressed as[11]:

$$\mathbf{FOM} = \frac{Power}{2^{ENOB} \times fs} \qquad (8)$$

This work presents an intermediate FOM value while its working speed is superior to most of other listed works, probably thanks to the proposed bootstrap switches and ways of lightening load capacitance.

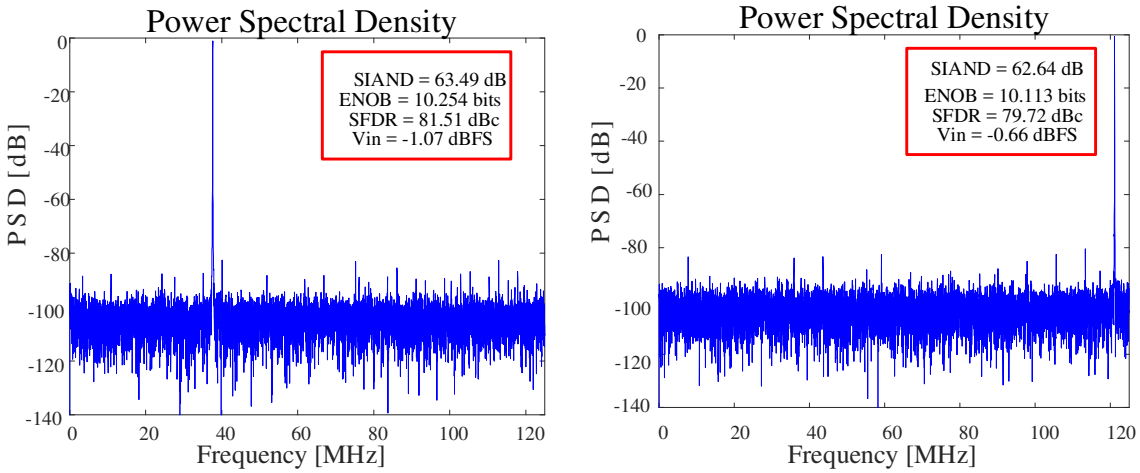

Figure 8 – Measured results with (a) 39.1MHz input @ 250 MS/s and (b) Nyquist input @ 250MS/s

Table 2 – ***Comparison with previous works***

Ref	8	1	9	10	This work (Measured)
Tech(nm)	180	180	130	130	130
Sampling rate (MHz)	100	250	270	100	250
Resolution (bit)	14	14	12	14	12
Supply (V)	1.8	1.8	1.2	1.2	1.3
Power (mW)	223	300	250	105	160
SFDR (dB)	91	88	77	/	81
SNDR (dB)	73	68	64	71	63
FOM (fj/conv)	540	570	740	360	555

Conclusions

We presented a 12 bit 250 MS/s pipeline ADC, designed and implemented on a 0.13 um CMOS process. A bootstrap switch with a buffer is proposed to improve the preceding stage's residue settling. Ways of lightening load capacitance are also used to speed up the RA. Clock generator with an improved timing is also introduced to increase the sampling linearity. The measurement results show that it can achieve 81 dB SFDR and 63 dB SNDR. The ADC core consumes 160 mW and obtains 555 fj/cov FOM.

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12-BIT 250 MS / S ОДНОКАНАЛЬНИЙ ТРУБОПРОВІДНИЙ АЦП З 81 DB SFDR IN 0,13 UM CMOS

Анотація. *АЦП трубопроводу з роздільною здатністю 12 Мбіт / с, представлений та виготовлений в процесі CMOS 0.13um. Для високошвидкісних міркувань пропонується енергозберігаючий перемикач з буфером. Він використовує вихідний пристрій для ізоляції підсилювача залишків та великого конденсатора в перемикачі завантажувача. Запропоновано методики освітлення ємності навантаження на кожній стадії, щоб прискорити відповідні підсилювачі залишків (RA). Тактовий генератор та оптимізований таймер запропоновані для досягнення низького джиттера та покращення лінійності вибірки, заощаджуючи більше часу для вхідного вимикача. Референтний буфер і годинниковий буфер повністю інтегровані. Співвідношення сигнал-спотворення та шуму (SNDR) оцінюється шляхом прийняття належної схеми та перевірки вимірюваними результатами. Виміряний сигнал SNDR становить 63 дБ, а брехні – вільний динамічний діапазон (SFDR) – 81 дБ з 39 МГц. Площа ядра становить 2 мм2, а АЦП споживає 160 мВт на 1,3 В.*

Ключові слова: трубопровідний АЦП; завантажувальні перемикачі; еталонний буфер; годинниковий буфер; терміни

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